In Re the Specification

Please replace the entire **DETAILED DESCRIPTION OF THE EMBODIMENTS** with the replacement section shown below. Both a marked version illustrating the changes to the **DETAILED DESCRIPTION OF THE EMBODIMENTS** section and a clean version have been provided.

Marked version illustrating changes

[0012] Referring now to the drawings, in which like numerals represent like elements or steps throughout the several views, FIG. 1 illustrates a block diagram representation of a system **100** that may contain a processor **105**, a memory controller **~~110~~130**, and a stacked memory array **115**, which may contain a first memory array **~~120~~110A** and a second memory array **~~120~~110B**. The memory controller **~~110~~130** may act as an interface to control the flow of data between the processor **105** and the stacked memory array **115**. The memory controller **~~110~~130** may be configured to sequence two write state machines **~~125~~105A** and **~~125~~105B** and to program the stacked memory array **115** having the first memory array **~~120~~110A** and the second memory array **~~120~~110B** in accordance with some embodiments of the present invention.

[0013] The first ~~M~~memory array **~~120~~110A** and the second memory array **~~120~~110B** may typically comprise arrays of memory cells. In an exemplary embodiment, the first memory array **~~120~~110A** and the second memory array **~~120~~110B** may be stacked vertically such that the second memory array **~~120~~110B** may be physically on top of the first memory array **~~120~~110A**. In an exemplary embodiment, the memory arrays **~~120~~110** may typically be NOR flash memory arrays; however, those skilled in the art will appreciate that other types of memory arrays, including but not limited to, NAND flash memory, random access memory ("RAM"), static random access memory ("SRAM"), and the like may be used without deviating from the scope of the embodiments of the present invention. Although the stacked memory array **115** may be

described in terms of two memory arrays, those skilled in the art will appreciate that the number of memory arrays ~~120~~**110** is not limited and may contain any number of individual memory arrays ~~120~~**110** without departing from the scope of the embodiments of the present invention.

[0014] In an exemplary embodiment, ~~T~~the write state machines ~~125~~**105A**, ~~125~~**105B** may be the internal controllers of the individual memory arrays **110A, 110B**, respectively. The write state machines ~~125~~**105A, 105B** may be operable to follow an algorithm to program the individual memory arrays ~~120~~**110** by using pulses of current from a pulse generator ~~130~~**120**.

[0015] The memory controller ~~110~~**130** may also include the~~a~~ pulse generator ~~130~~**120** that ~~may be~~is operable to generate a waveform containing a series of current pulses, which may be supplied to the write state machines ~~125~~**105A, 105B**. The pulse generator ~~130~~**120** ~~may~~ also communicates with a delay circuit ~~135~~**125** that ~~may be~~is operable to inject a time delay between a first pulse of current applied to the first write state machine ~~125~~**105A** and a second pulse of current applied to the second write state machine ~~125~~**105B**.

[0016] FIG. 2 illustrates a ~~prior art~~ waveform **200** including a plurality of pulses of current that may be generated by the pulse generator ~~130~~**120** and applied to the write state machines ~~125~~**105A, 105B**. The waveform **200** may begin, in time, with a short initial pulse **205** of current having a large amplitude, which may ~~typically~~ be used to initiate a write or erase operation to the individual memory cell and also to supply the majority of the current to the cell of the stacked memory array ~~120~~**115**. In an exemplary embodiment, the initial pulse **205** may have an amplitude of 25.4 milliamperes for approximately 1 microsecond, and may have a pulse width of approximately 2 microseconds.

[0017] After the initial pulse **205**, there may be a period of time, or a delay **210**, during which time the system **100** may read what current is on each cell of the stacked memory array ~~**120A**~~**115**. In an exemplary embodiment, the delay **210** may be approximately 7 microseconds long at 3 milliamperes. After the delay **210**, there may be a second pulse **215**, which may be used to supply additional current to the write state machine **105A, 105B**. Unlike the initial pulse **205**, this second pulse **215** may have a peak amplitude that is less than the pulse amplitude of the initial pulse **205**. In an exemplary embodiment, the peak amplitude may have a plateau at 10.6 milliamperes and a pulse width of approximately 30 microseconds, with a rise time of approximately 2 microseconds. After this second pulse **215**, there may be a plurality of additional brief delays **220** with smaller pulses **225** therebetween. In an exemplary embodiment, the plurality of brief delays **220** with smaller pulses **225** therebetween may include three brief delays **220** and three pulses **225**. During the brief delays **220** the system **100** may read the voltage on the individual cells of the stacked memory array ~~**120A**~~**115**. Each brief delay **220** may last for approximately 2 microseconds at about 4 milliamperes. The three pulses **225** may indicate when additional current is being supplied to the write state machine **125**. Each of the three pulses **225** may last for approximately 22 microseconds at 10.6 milliamperes.

[0018] After the plurality of additional brief delays **220** and pulses **225**, there may be a second delay **230**, which may permit the system **100** to verify if there is enough voltage on each cell of the stacked memory array ~~**120A**~~**115**. The second delay **230**, in an exemplary embodiment, may last for about 20 microseconds at 2 milliamperes. If the memory controller ~~**110**~~**130** determines that enough voltage has not been built up within the memory cell, then an additional plurality of pulses **225**, which are shown in the dashed line in the figure, may be

generated by the pulse generator ~~130~~120 to increase the voltage on the cells of the stacked memory array ~~120A~~115 to the appropriate value.

[0019] Although ~~an exemplary prior art~~ waveform **200** h~~aving a plurality of pulses therein~~ has been described as having certain properties, including amplitudes and durations of individual pulses, those skilled in the art will appreciate that pulses of current having other amplitudes and durations, may be applied individually or in combination to the write state machines ~~125~~**105A, 105B**, which may create other waveforms that are within the scope of the embodiments of the present invention. For example, another waveform within the scope of the embodiments of the present invention may have a series of pulses therein, wherein all pulses may be of equal amplitude, duration, and period, such as the waveforms depicted in FIG. 6.

~~[0020]~~FIG. 3 is a logical flow diagram illustrating a routine **300** of sequencing multiple write state machines ~~125~~**105A, 105B** according to some embodiments of the present invention. Starting at **310**, the pulse generator ~~130~~**120** may apply current, in the form of ~~the~~a first initial pulse ~~205A~~, to the first write state machine ~~125~~**105A**. At **320**, the delay circuit ~~135~~**125** may inject a time-delay **Δt** into the system **100** so that ~~the~~a initial pulse ~~205B~~ applied to the second write state machine ~~125~~**105B** may occur ~~during the time of the delay 210A of~~ after the first initial pulse is supplied to the first write state machine ~~125~~**105A** in accordance with an exemplary embodiment of the present invention.

~~[0021]~~In an alternative ~~second~~ exemplary embodiment, at **320**, the delay circuit ~~135~~**125** may inject a time-delay **Δt** into the system **100** so that the initial pulse ~~205B~~ applied to the second write state machine ~~125~~**105B** may occur during the time of the delay ~~230A~~ between the first plurality of three brief delays ~~220A~~ and pulses ~~225A~~ and the second plurality of brief delays

~~**220A**~~ and pulses ~~**225A**~~ applied to the first write state machine **125A**. ~~By applying the initial pulse **205B** during either the delay **210A** or the delay **230A**, the peaks of the initial pulses **205A** and **205B** may not align in time, thereby allowing the system **100** to accommodate all current without incorporating a larger voltage regulator.~~

~~[0011]~~[0020] Then at **330**, the pulse generator ~~**130**~~**120** may apply current to the next write state machine **105**, which in an exemplary embodiment may be the second write state machine **105B**. In an exemplary embodiment, the amount of time-delay **Δt** may be at least as long as the amount of time of the first initial pulse ~~**205**~~ applied to the first write state machine **105A** ~~of the first waveform **200A**~~ so as to prevent the initial pulses ~~**205**~~ applied to the first write state machine **105A**~~, in the form of the waveform **200**, generated by the pulse generator **130**~~ from occurring simultaneously or during the rise and fall interval of the first initial pulse ~~**205**~~ applied to the second ~~first~~ write state machine **105**~~**A**~~**B**. Thus, in an exemplary embodiment, the second waveform may be offset from the first waveform by at least 2 microseconds. This may assure that the initial pulses ~~**205** of the first waveform **200A** and the second waveform **200B**~~ applied to the first write state machine **105A** and the second write state machine **105B** do not line up, thereby minimizing the amount of current needed to generate waveforms **200** to the first and second memory arrays ~~**120**~~**110A**, ~~**120**~~**110B**.

~~[0012]~~[0021] Although the routine **300** has been described with respect to two write state machines ~~**125**~~**105 A, 105B**, those skilled in the art will appreciate that the routine **300** may be applied to any number of write state machines ~~**125**~~, such that there may be a time-delay **Δt** between subsequent pulses of current applied to subsequent write state machines ~~**125**~~**105A, 105B**.

~~[0013]~~[0022] FIG. 4 is a timing diagram illustrating a pair of current waveforms ~~200~~**400A**, ~~200~~**400B** for programming the~~a~~ stacked memory array **115** in accordance with one embodiment of the present invention. In an exemplary embodiment, the pulse generator ~~130~~**120** may apply the first pulse ~~205~~**405A** of current of the plurality of pulses, which together may form the first waveform ~~200~~**400A**, to the first write state machine ~~125~~**105A**. Then, the delay circuit ~~135~~**125** may inject a time-delay **Δt** 407 before the pulse generator ~~130~~**120** may apply a first pulse ~~205~~**405B** of the plurality of pulses, which together may form the second waveform ~~200~~**400B**, to the second write state machine ~~125~~**105B**. Thus, in an exemplary embodiment, the initial pulse ~~205~~**405A** of the first waveform ~~200~~**400A** may be applied to the first write state machine ~~125~~**105A** and then the initial pulse ~~205~~**405B** of the second waveform ~~200~~**400B** may be applied to the second write state machine ~~125~~**105B** at a time of at least 2 microseconds after the initial pulse ~~205~~**405A** of the first waveform ~~200~~**400A**. Therefore, in an exemplary embodiment, the second initial pulse ~~205~~**405B** may occur during the time of the first delay ~~210~~**410** of the first waveform ~~200~~**400A**, and thus, in an exemplary embodiment, the second waveform ~~200~~**400B** may be delayed a period equal to **Δt** 407. Those skilled in the art will appreciate that the length of the time-delay **Δt** 407 between the first waveform ~~200~~**400A** and the second waveform ~~200~~**400B** may be in the range of microseconds so that the entire second initial pulse ~~205~~**405B** may occur during the first delay ~~210~~**410** in the waveform ~~200~~**400A** having a plurality of pulses applied to the first write state machine ~~125~~**105A.**

~~[0014]~~[0023] FIG. 5 is a timing diagram illustrating a pair of current waveforms ~~200~~**500A**, ~~200~~**500B** for programming a stacked memory array **115** in accordance with another embodiment of the present invention. In an exemplary embodiment, the pulse generator ~~130~~**120** may apply the first pulse ~~205~~**505A** of current of the plurality of pulses, which together may form the first

waveform **~~200~~505A**, to the first write state machine **~~125~~105A**. Then, the delay circuit **~~135~~125** may inject a time-delay **Δt 507** before the pulse generator **~~130~~120** may apply a first pulse **~~205~~505B** of the plurality of pulses, which together may form the second waveform **~~200~~500B**, to the second write state machine **~~125~~105B**. Thus, the initial pulse **~~205~~505A** of the first waveform **~~200~~505A** may be applied to the first write state machine **~~125~~105A** and then the initial pulse **~~205~~505B** of the second waveform **~~200~~500B** may be applied to the second write state machine **~~125~~105B** at some time after the initial pulse **~~205~~505A** of the first waveform **~~200~~500A**. Therefore, in an exemplary embodiment, the second initial pulse **~~205~~505B** may occur during the time of the second delay **~~230~~530** of the first waveform **~~200~~500A**, and thus, in an exemplary embodiment, the second waveform **~~200~~500B** may be delayed a period equal to **Δt 507**. Those skilled in the art will appreciate that the length of time the second waveform **~~200~~500B** may be delayed may be in the range of 93 microseconds to 111 microseconds so that the entire second initial pulse **~~205~~505B** may occur during the second delay **~~230~~530** in the waveform **~~200~~500A** having a plurality of pulses applied to the first write state machine **~~125~~105A.**

~~[0015]~~[0024] Also, those skilled in the art will appreciate the length of time that the second waveform **~~200~~500B** may be delayed may be other amounts of time so long as that when the total amount of current in the system **100** is aggregated, the voltage regulator may accommodate the aggregated current. Thus, it may be within the scope of the embodiments of the present invention to delay the second initial pulse **~~205~~505B** that may be applied to the second write state machine **~~125~~105B** such that a portion of the second initial pulse **~~205~~505B** may overlap a portion of the first initial pulse **~~205~~505A** that may be applied to the first write state machine **~~125~~105A**. Because in some exemplary embodiments, the peak amplitudes of the two initial pulses **~~205~~505A**

and **505B** may not occur simultaneously, a standard voltage regulator may accommodate the total current of the system **100** at any given time.

~~[0016]~~[0025] In exemplary embodiments, the time delay **Δt 507** between the first waveform ~~**200**~~**500A** and the second waveform ~~**200**~~**500B** may be between 2 and 111 microseconds, which may create a minimal delay in the amount of time the system **100** requires to program the stacked memory arrays ~~**120**~~**115**, as compared to the seconds added if the write state machines ~~**125**~~**105** were to be programmed sequentially. Additionally, by creating a time-delay **Δt 507** between the two waveforms ~~**200**~~**505A** and **505B** applied to the two write state machines ~~**125**~~**105**, the overall cost of manufacturing and operating the system **100** may decrease as compared to the cost of manufacturing and operating a system in which the write state machines ~~**125**~~**105** are programmed in parallel (i.e., simultaneously). This is due in part to the fact that in many cases, a new regulator should be added to the system to accommodate the larger amounts of current and in part to the fact that a lesser amount of current may be applied simultaneously.

~~[0017]~~[0026] FIG. 6 is a timing diagram illustrating a pair of current waveforms **600A** and **600B** for programming a stacked memory array **115** in accordance with still another embodiment of the present invention. Waveforms **600A** and **600B** may include a series of pulses **605** therein wherein all pulses **605** may be of equal amplitude, duration, and period. In an exemplary embodiment, the pulse generator ~~**130**~~**120** may apply the first pulse **605A**$_1$ of current of the first waveform **600A**, to the first write state machine ~~**125**~~**105A**. Then, the delay circuit ~~**135**~~**125** may inject a time-delay **Δt** before the pulse generator ~~**130**~~**120** may apply a first pulse **605B**$_1$ of current of the second waveform **600B** to the second write state machine ~~**125**~~**105B**. Therefore, in an exemplary embodiment, the second initial pulse **605B**$_1$ may occur during the time of a first delay

$610A_1$ of the first waveform **600A**, and thus, in an exemplary embodiment, the second waveform **600B** may be delayed a period equal to **Δt**.

[0027] Other alternative embodiments will become apparent to those skilled in the art to which an exemplary embodiment pertains without departing from its spirit and scope. Accordingly, the scope of the embodiments of the present invention may be defined by the appended claims rather than the foregoing description.

Clean version

[0012] Referring now to the drawings, in which like numerals represent like elements or steps throughout the several views, FIG. 1 illustrates a block diagram representation of a system **100** that may contain a processor **105**, a memory controller **130**, and a stacked memory array **115**, which may contain a first memory array **110A** and a second memory array **110B**. The memory controller **130** may act as an interface to control the flow of data between the processor **105** and the stacked memory array **115**. The memory controller **130** may be configured to sequence two write state machines **105A** and **105B** and to program the stacked memory array **115** having the first memory array **110A** and the second memory array **110B** in accordance with some embodiments of the present invention.

[0013] The first memory array **110A** and the second memory array **110B** may typically comprise arrays of memory cells. In an exemplary embodiment, the first memory array **110A** and the second memory array **110B** may be stacked vertically such that the second memory array **110B** may be physically on top of the first memory array **110A**. In an exemplary embodiment, the memory arrays **110** may typically be NOR flash memory arrays; however, those skilled in the art will appreciate that other types of memory arrays, including but not limited to, NAND flash

memory, random access memory ("RAM"), static random access memory ("SRAM"), and the like may be used without deviating from the scope of the embodiments of the present invention. Although the stacked memory array **115** may be described in terms of two memory arrays, those skilled in the art will appreciate that the number of memory arrays **110** is not limited and may contain any number of individual memory arrays **110** without departing from the scope of the embodiments of the present invention.

[0014] In an exemplary embodiment, the write state machines **105A, 105B** may be the internal controllers of the individual memory arrays **110A, 110B**, respectively. The write state machines **105A, 105B** may be operable to follow an algorithm to program the individual memory arrays **110** by using pulses of current from a pulse generator **120**.

[0015] The memory controller **130** may also include the pulse generator **120** that is operable to generate a waveform containing a series of current pulses, which may be supplied to the write state machines **105A, 105B**. The pulse generator **120** also communicates with a delay circuit **125** that is operable to inject a time delay between a first pulse of current applied to the first write state machine **105A** and a second pulse of current applied to the second write state machine **105B**.

[0016] FIG. 2 illustrates a waveform **200** including a plurality of pulses of current that may be generated by the pulse generator **120** and applied to the write state machines **105A, 105B**. The waveform **200** may begin, in time, with a short initial pulse **205** of current having a large amplitude, which may be used to initiate a write or erase operation to the individual memory cell and also to supply the majority of the current to the cell of the stacked memory array **115**. In an exemplary embodiment, the initial pulse **205** may have an amplitude of 25.4

milliamperes for approximately 1 microsecond, and may have a pulse width of approximately 2 microseconds.

[0017] After the initial pulse **205**, there may be a period of time, or a delay **210**, during which time the system **100** may read what current is on each cell of the stacked memory array **115**. In an exemplary embodiment, the delay **210** may be approximately 7 microseconds long at 3 milliamperes. After the delay **210**, there may be a second pulse **215**, which may be used to supply additional current to the write state machine **105A, 105B**. Unlike the initial pulse **205**, this second pulse **215** may have a peak amplitude that is less than the pulse amplitude of the initial pulse **205**. In an exemplary embodiment, the peak amplitude may have a plateau at 10.6 milliamperes and a pulse width of approximately 30 microseconds, with a rise time of approximately 2 microseconds. After this second pulse **215**, there may be a plurality of additional brief delays **220** with smaller pulses **225** therebetween. In an exemplary embodiment, the plurality of brief delays **220** with smaller pulses **225** therebetween may include three brief delays **220** and three pulses **225**. During the brief delays **220** the system **100** may read the voltage on the individual cells of the stacked memory array **115**. Each brief delay **220** may last for approximately 2 microseconds at about 4 milliamperes. The three pulses **225** may indicate when additional current is being supplied to the write state machine **125**. Each of the three pulses **225** may last for approximately 22 microseconds at 10.6 milliamperes.

[0018] After the plurality of additional brief delays **220** and pulses **225**, there may be a second delay **230**, which may permit the system **100** to verify if there is enough voltage on each cell of the stacked memory array **115**. The second delay **230**, in an exemplary embodiment, may last for about 20 microseconds at 2 milliamperes. If the memory controller **130** determines that enough voltage has not been built up within the memory cell, then an additional plurality of

pulses **225**, which are shown in the dashed line in the figure, may be generated by the pulse generator **120** to increase the voltage on the cells of the stacked memory array **115** to the appropriate value.

[0019] Although waveform **200** h has been described as having certain properties, including amplitudes and durations of individual pulses, those skilled in the art will appreciate that pulses of current having other amplitudes and durations, may be applied individually or in combination to the write state machines **105A, 105B**, which may create other waveforms that are within the scope of the embodiments of the present invention. For example, another waveform within the scope of the embodiments of the present invention may have a series of pulses therein, wherein all pulses may be of equal amplitude, duration, and period, such as the waveforms depicted in FIG. 6.

[0020] FIG. 3 is a logical flow diagram illustrating a routine **300** of sequencing multiple write state machines **105A, 105B** according to some embodiments of the present invention. Starting at **310**, the pulse generator **120** may apply current, in the form of a first initial pulse, to the first write state machine **105A**. At **320**, the delay circuit **125** may inject a time-delay **Δt** into the system **100** so that a initial pulse applied to the second write state machine **105B** may occur after the first initial pulse is supplied to the first write state machine **105A** in accordance with an exemplary embodiment of the present invention. In an alternative exemplary embodiment, at **320**, the delay circuit **125** may inject a time-delay **Δt** into the system **100** so that the initial pulse applied to the second write state machine **105B** may occur during the time of the delay between the first plurality of three brief delays and pulses and the second plurality of brief delays and pulses applied to the first write state machine **125A**. Then at **330**, the pulse generator **120** may apply current to the next write state machine, which in an exemplary embodiment may be the

second write state machine **105B**. In an exemplary embodiment, the amount of time-delay **Δt** may be at least as long as the amount of time of the first initial pulse applied to the first write state machine **105A** so as to prevent the initial pulse applied to the first write state machine **105A** from occurring simultaneously or during the rise and fall interval of the first initial pulse applied to the second write state machine **105B**. Thus, in an exemplary embodiment, the second waveform may be offset from the first waveform by at least 2 microseconds. This may assure that the initial pulses applied to the first write state machine **105A** and the second write state machine **105B** do not line up, thereby minimizing the amount of current needed to generate waveforms **200** to the first and second memory arrays **110A, 110B**.

[0021] Although the routine **300** has been described with respect to two write state machines **105**, those skilled in the art will appreciate that the routine **300** may be applied to any number of write state machines **105A, 105B**, such that there may be a time-delay **Δt** between subsequent pulses of current applied to subsequent write state machines **105**.

[0022] FIG. 4 is a timing diagram illustrating a pair of current waveforms **400A, 400B** for programming the stacked memory array **115** in accordance with one embodiment of the present invention. In an exemplary embodiment, the pulse generator **120** may apply the first pulse **405A** of current of the plurality of pulses, which together may form the first waveform **400A**, to the first write state machine **105A**. Then, the delay circuit **125** may inject a time-delay **Δt 407** before the pulse generator **120** may apply a first pulse **405B** of the plurality of pulses, which together may form the second waveform **400B**, to the second write state machine **105B**. Thus, in an exemplary embodiment, the initial pulse **405A** of the first waveform **400A** may be applied to the first write state machine **105A** and then the initial pulse **405B** of the second

waveform **400B** may be applied to the second write state machine **105B** at a time of at least 2 microseconds after the initial pulse **405A** of the first waveform **400A**. Therefore, in an exemplary embodiment, the second initial pulse **405B** may occur during the time of the first delay **410** of the first waveform **400A**, and thus, in an exemplary embodiment, the second waveform **400B** may be delayed a period equal to **Δt 407**. Those skilled in the art will appreciate that the length of the time-delay **Δt 407** between the first waveform **400A** and the second waveform **400B** may be in the range of microseconds so that the entire second initial pulse **405B** may occur during the first delay **410** in the waveform **400A** having a plurality of pulses applied to the first write state machine **105A.**

[0023] FIG. 5 is a timing diagram illustrating a pair of current waveforms **500A, 500B** for programming a stacked memory array **115** in accordance with another embodiment of the present invention. In an exemplary embodiment, the pulse generator **120** may apply the first pulse **505A** of current of the plurality of pulses, which together may form the first waveform **505A**, to the first write state machine **105A**. Then, the delay circuit **125** may inject a time-delay **Δt 507** before the pulse generator **120** may apply a first pulse **505B** of the plurality of pulses, which together may form the second waveform **500B**, to the second write state machine **105B**. Thus, the initial pulse **505A** of the first waveform **505A** may be applied to the first write state machine **105A** and then the initial pulse **505B** of the second waveform **500B** may be applied to the second write state machine **105B** at some time after the initial pulse **505A** of the first waveform **500A**. Therefore, in an exemplary embodiment, the second initial pulse **505B** may occur during the time of the second delay **530** of the first waveform **500A**, and thus, in an exemplary embodiment, the second waveform **500B** may be delayed a period equal to **Δt 507**. Those skilled in the art will appreciate that the length of time the second waveform **500B** may be

delayed may be in the range of 93 microseconds to 111 microseconds so that the entire second initial pulse **505B** may occur during the second delay **530** in the waveform **500A** having a plurality of pulses applied to the first write state machine **105A.**

[0024] Also, those skilled in the art will appreciate the length of time that the second waveform **500B** may be delayed may be other amounts of time so long as that when the total amount of current in the system **100** is aggregated, the voltage regulator may accommodate the aggregated current. Thus, it may be within the scope of the embodiments of the present invention to delay the second initial pulse **505B** that may be applied to the second write state machine **105B** such that a portion of the second initial pulse **505B** may overlap a portion of the first initial pulse **505A** that may be applied to the first write state machine **105A**. Because in some exemplary embodiments, the peak amplitudes of the two initial pulses **505A** and **505B** may not occur simultaneously, a standard voltage regulator may accommodate the total current of the system **100** at any given time.

[0025] In exemplary embodiments, the time delay **Δt 507** between the first waveform **500A** and the second waveform **500B** may be between 2 and 111 microseconds, which may create a minimal delay in the amount of time the system **100** requires to program the stacked memory arrays **115**, as compared to the seconds added if the write state machines **105** were to be programmed sequentially. Additionally, by creating a time-delay **Δt 507** between the two waveforms **505A** and **505B** applied to the two write state machines **105**, the overall cost of manufacturing and operating the system **100** may decrease as compared to the cost of manufacturing and operating a system in which the write state machines **105** are programmed in parallel (i.e., simultaneously). This is due in part to the fact that in many cases, a new regulator

should be added to the system to accommodate the larger amounts of current and in part to the fact that a lesser amount of current may be applied simultaneously.

[0026] FIG. 6 is a timing diagram illustrating a pair of current waveforms **600A** and **600B** for programming a stacked memory array **115** in accordance with still another embodiment of the present invention. Waveforms **600A** and **600B** may include a series of pulses **605** therein wherein all pulses **605** may be of equal amplitude, duration, and period. In an exemplary embodiment, the pulse generator **120** may apply the first pulse **$605A_1$** of current of the first waveform **600A**, to the first write state machine **105A**. Then, the delay circuit **125** may inject a time-delay **Δt** before the pulse generator **120** may apply a first pulse **$605B_1$** of current of the second waveform **600B** to the second write state machine **105B**. Therefore, in an exemplary embodiment, the second initial pulse **$605B_1$** may occur during the time of a first delay **$610A_1$** of the first waveform **600A**, and thus, in an exemplary embodiment, the second waveform **600B** may be delayed a period equal to **Δt**.

[0027] Other alternative embodiments will become apparent to those skilled in the art to which an exemplary embodiment pertains without departing from its spirit and scope. Accordingly, the scope of the embodiments of the present invention may be defined by the appended claims rather than the foregoing description.